ACS APPLIED MATERIALS & INTERFACES

RESEARCH ARTICLE

www.acsami.org

A Simple Device Unit Consisting of All NiO Storage and Switch Elements for Multilevel Terabit Nonvolatile Random Access Memory

Myoung-Jae Lee,*,† Seung-Eon Ahn,†,‡ Chang Bum Lee,† Chang-Jung Kim,† Sanghun Jeon,† U-In Chung,† In-Kyeong Yoo,† Gyeong-Su Park,§ Seungwu Han,⊥ In Rok Hwang,# and Bae-Ho Park*,#

†Semiconductor Device Laboratory and §Analytical Research Laboratory, Samsung Advanced Institute of Technology, Gyeonggi 440-600, Korea

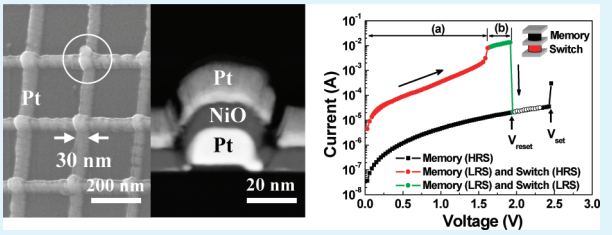
‡School of Electrical Engineering, Korea University, Seoul 136-701, Korea

⊥Department of Materials Science and Engineering, Seoul National University, Seoul 151-744, Korea

#Division of Quantum Phases & Devices, Department of Physics, Konkuk University, Seoul 143-701, Korea

Supporting Information

ABSTRACT: Present charge-based silicon memories are unlikely to reach terabit densities because of scaling limits. As the feature size of memory shrinks to just tens of nanometers, there is insufficient volume available to store charge.[1] Also, process temperatures higher than 800 °C make silicon incompatible with three-dimensional (3D) stacking structures. Here we present a device unit consisting of all NiO storage and switch elements for multilevel terabit nonvolatile random access memory using resistance switching.[2−5] It is demonstrated that NiO films are scalable to around 30 nm and compatible with multilevel cell technology. The device unit can be a building block for 3D stacking structure because of its simple structure and constituent, high performance, and process temperature lower than 300 °C. Memory resistance switching of NiO storage element is accompanied by an increase in density of grain boundary while threshold resistance switching of NiO switch element is controlled by current flowing through NiO film.



KEYWORDS: resistance random access memory (ReRAM), multilevel terabit memory, 3D-stacking structure, memory element, switch element

INTRODUCTION

The lithographic scaling limits of the current champion of high density nonvolatile memory, Flash, will soon reach its scaling limit around 20 nm.[1] In general, one can increase device density by scaling down the size or by using multilevel cell (MLC) in order to store more than one bit of information per device. More recently, three-dimensional (3D) stacking has been proposed and shown to be possible.[6] To reach extreme high density such as terabit, it is required to utilize scale down, MLC, and 3D cell stacking technologies at the same time.

In general, nonvolatile random access memory cell is consisting of storage and switch elements. Scale down technology must be compatible with both elements while MLC technology is only applied to storage element. Because 3D cell stacking technology involves reproducible stacking of memory cells, simple cell structure, and constituent materials as well as low-temperature process are necessary. If a scalable low-temperature processed material revealing MLC characteristics can be used in both storage and switch elements with simple $4F^2$ (F: minimum feature size) structure, it can be one of the best candidate materials applicable to terabit nonvolatile random access memory.

Transition metal oxides (TMOs) have recently been studied for applications in next generation electrical and optical devices.[2−4,7−9] Since early research in the resistance switching properties of transition metal oxides, two distinct types of electrical switching have been well-known: bistable (or nonvolatile memory) switching[10−15] and monostable (or volatile threshold) switching.[16−20] Each type of switching has applications suitable for memory device components.[9] Nonvolatile memory switching can be applied toward storage elements.[9,18] Meanwhile volatile threshold switching has been shown to be useful as a two terminal bidirectional switch element similar to a Zener diode.[18] Several oxide materials have shown both types of switching depending on fabrication method and measurement conditions.[11,12,19] In particular, NiO can be fabricated to show either type of switching behavior.

In this paper, we report high performance of a nonvolatile random access memory cell consisting of all NiO storage and switch elements with simple $4F^2$ capacitor structure. By using homogeneous material for both elements and reducing the vertical size of the switch element, we can achieve more stable and continuous process than that used to fabricate others including poly Si or oxide diode.[6,7] Moreover, our NiO capacitor structure is scalable to ~$(30\ \text{nm})^2$ and applicable

Received: August 29, 2011
Accepted: October 11, 2011
Published: October 11, 2011

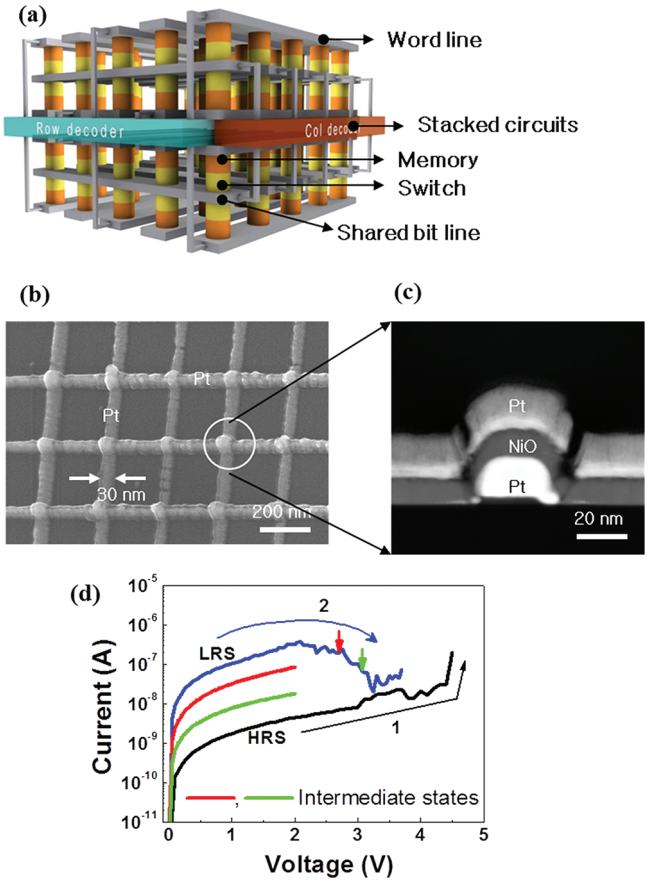


Figure 1. Scalability and compatibility with MLC technology. (a) Conceptual diagram for ideal 3-dimensional stacking structure of memory cells and peripheral circuits. (b) A 3 × 5 Pt-NiO-Pt crossbar memory array with 30 nm feature size. (c) Cross-sectional STEM image of Pt-NiO-Pt memory cell. (d) Operation of a 30 nm × 30 nm memory cell showing nonvolatile memory resistance switching. Intermediate states are also available by appropriate control of sweep voltage during changes from LRS to HRS.

to MLC. Previous reports on NiO memory element have demonstrated several parameters such as endurance up to 1×10^6 cycles, read cycles up to 10^{12} cycles, retention up to 5 months at room temperature and switching at temperature up to 300 °C.[21] In addition to the excellent performances reported in previous works,[18,21,22] we first show stable operation of NiO memory element at 30 nm as well as MLC levels which appear in nanoscale.

EXPERIMENTAL SECTION

Preparation of 30 nm Sized Devices. E-beam lithography was used to define crossbar cell structures including NiO films with 30 nm feature size. First, a two-layered electroresist (ER) fabrication process was used to create Pt/Ti bottom electrode lines (30 nm thick.) on the SiO_2 substrates. The two ER layers were composed of ZEP-520A7 from ZEONREX Electronic Chemicals on top of lift-off resist 1A (LOR1A) from Microchem Corp. (see the Supporting Information, Figure S1). This method was used to define a more precise cell structure and get higher device yield. Pt/Ti was deposited using e-beam evaporation on the bottom lines formed by electron-beam lithography and then patterned using a lift-off method. NiO film with 20 nm thickness was deposited by reactive DC magnetron sputtering using a Ni target at 5% partial oxygen ratio of (argon + oxygen) gas mixture and 300 °C. Thirty nanometer thick Pt top electrodes were deposited using the same process with the bottom electrodes using an alignment mark to create the crossbar structure.

Fabrication of a Device with All NiO Storage and Switch Elements. We deposited NiO films on Pt bottom electrodes by reactive DC magnetron sputtering of either Ni or Li-doped (0.05 wt %) Ni targets at 5−30% partial oxygen ratio of (argon + oxygen) gas mixture at 300 °C. By varying the partial oxygen ratio, we could fabricate both types of switching (volatile threshold and nonvolatile memory) NiO films. Conventional photolithography was used to define Pt top electrodes with 30 μm feature size.

Electrical Measurements. DC electrical characterizations were performed using Agilent 4156C semiconductor analyzer in voltage and current sweep modes. Current compliance was used to limit the maximum current passing through the device during voltage sweep.

RESULTS AND DISCUSSION

A conceptual diagram of a terabit nonvolatile random access memory device is shown in Figure 1a. Storage elements made of TMOs and especially NiO are advantageous for stacking structures due to their relatively low deposition and processing temperatures.[9] Additionally a scanning electron microscopy (SEM) image of our crossbar memory array of Pt-NiO-Pt devices with 30 nm feature size is demonstrated in Figure 1b, with a cross-sectional scanning transmission electron microscopy (STEM) image of single device shown in Figure 1c (see Method section and Figure S1 in the Supporting Information).

Confirmation of the nonvolatile memory switching at a Pt-NiO-Pt device with 30 nm feature size by voltage sweep measurement is shown in Figure 1d. The device starts at high resistance state (HRS) labeled 1; however, upon reaching around 4.5 V, an abrupt increase in current is observed. The total current flow through the device is limited externally by a compliance current of 0.2 μA as previously reported.[12] On the following voltage sweep, the device stays at low resistance state (LRS) labeled 2, and the HRS can be restored at around 3.2 V.

In addition, we confirm that our Pt-NiO-Pt device with 30 nm feature size can be applied to MLC. We can achieve stable intermediate states by controlling the stopping voltages during the sweep labeled 2, similar to previous reports.[23] The states denoted by red and green lines can be obtained by stopping voltages shown by the red and green arrows, respectively, during the sweep labeled 2. More than 90% of our Pt-NiO-Pt devices with 30 nm feature size show nonvolatile memory switching behavior and around 30% of them are MLCs.

To more easily fabricate samples for further experiments, Pt-NiO-Pt devices with cycling endurance values greater than 1×10^6 at 30 × 30 um^2 cell sizes have been used for following measurements. NiO is a well-known metal-deficient p-type semiconductor due to both Ni vacancies and compensating holes inside NiO films.[12] The oxygen partial pressure during reactive sputtering has been shown as a key parameter for determining the switching properties of NiO films.[3,12,18] Also, impurity doping can similarly be used in controlling electrical switching type. Figure 2a shows the DC resistivity measured by 2-point probe. The closed squares show experimental data from NiO samples deposited with oxygen partial pressures from 3 to 30%. NiO samples deposited with oxygen partial pressure of around 5% showed nonvolatile memory switching with relatively high resistivity at HRS while those deposited with oxygen partial pressure of 15−30% exhibited volatile threshold switching with

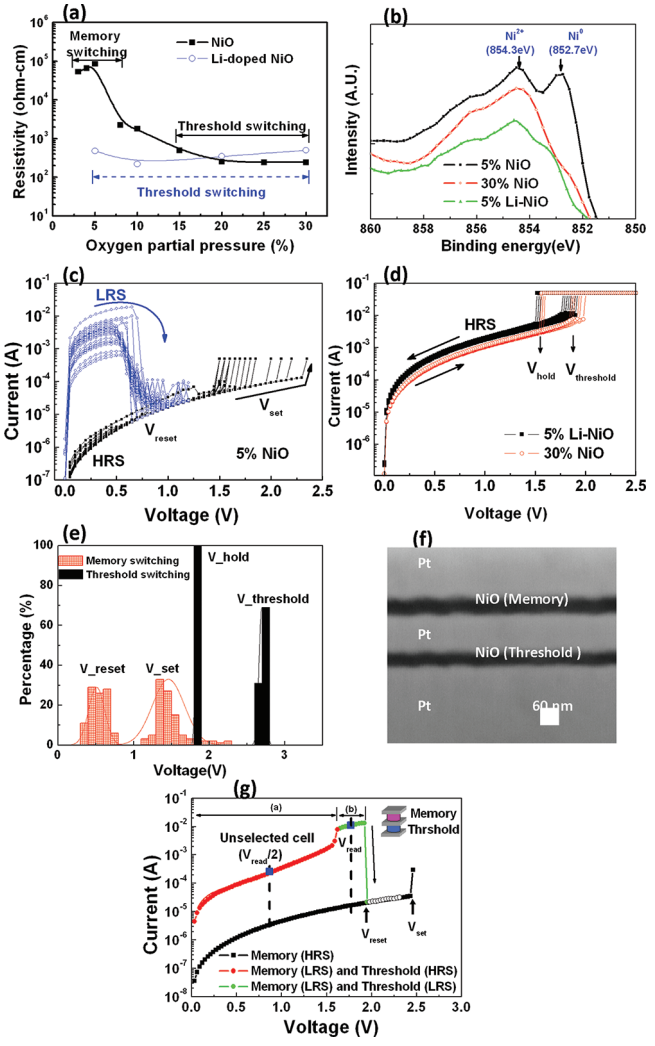


Figure 2. Dual function of NiO. (a) Resistivity data obtained at 0.3 V from NiO and Li-doped NiO films fabricated at different oxygen partial pressure. Memory and threshold switching regions are indicated. (b) Ni $2p_{3/2}$ core level XPS spectrum of the 5% NiO, 30% NiO, and 5% Li-NiO films. (c) 50 cycles of memory switching for 5% NiO and d) 50 cycles of threshold switching for 30% NiO and 5% Li-NiO films. (e) Distribution showing reset and set voltages for memory switching compared to threshold and hold voltages for threshold switching. (f) Cross-sectional STEM image and (g) resistance switching characteristics of a Pt-30% NiO-Pt-5% NiO-Pt device.

relatively low resistivity at HRS.[12] Meanwhile the open circles denote experimental data from Li-doped NiO samples deposited with oxygen partial pressure from 5 to 30%. All the Li-doped samples showed only threshold switching and similar resistivity values. X-ray photoelectron spectroscopy data in Figure 2b demonstrate the presence of metallic Ni, at 852.7 eV, in the NiO sample deposited with 5% oxygen partial pressure (5% NiO). We believe that this metallic Ni content plays an important role in nonvolatile memory switching, perhaps directly related to formation of conducting filaments.[3]

Figures 2c and d show repetitive 50 cycles of memory switching for a 5% NiO, and threshold switching for a NiO deposited with 30% oxygen partial pressure (30% NiO) and a Li-doped NiO deposited with 5% oxygen partial pressure (5% Li-NiO), respectively. For memory switching, V_{set} and V_{reset} correspond to switching voltages to LRS and HRS, respectively. For threshold switching, $V_{threshold}$ and V_{hold} are the highest and lowest voltages between which LRS is stable, respectively. $V_{threshold}$ and V_{hold} show much smaller distributions than those of V_{set} and V_{reset} as shown in Figure 2e. We believe that the mechanism behind the two different switching must be different for such an experimental result.

To verify the capabilities of 5 and 30% NiO films as storage and switch elements, respectively, we have fabricated a single device with stacking structures as previously reported.[24] Figure 2f shows the STEM cross-section image of the Pt-30% NiO-Pt-5% NiO-Pt device. (for more detailed HR-TEM, see Figure S2 in the Supporting Information) Device characteristics and operations are exhibited in Figure 2g. At voltages below 1.6 V labeled as region a, the switch element at HRS limits any operation of the device. In region (b), the cell can be accessed and stored information can be read by applying an appropriate reading voltage (V_{read}) from 1.6 to 2 V. Write operations can be performed at voltages between 2 and 2.5 V. For any crossbar array of such devices we access a single cell exclusively without interference with neighboring cells by V_{read} voltages to the cell while keeping voltage below threshold voltage of 1.6 V for the other cells. In the combined structure memory and switch element, the LRS current level or leakage current of the unselected cells using a $V_{read}/2$ scheme (unselected cells are biased at $V_{read}/2$) was decreased by the order of one as shown in Figure 2g.

Structural changes during memory and threshold switching have been examined by cross-sectional HR-TEM measurements. Figures 3a and b show HR-TEM images of 5% NiO film before and after applying V_{set} to the top electrode. Density of grain boundaries immensely increase after applying V_{set}. Higher-resolution image near grain boundary reveals that the width of grain boundary is less than 1 nm, as shown in Figure 3c. Figure 3d exhibits the magnified atomic resolution HR-TEM image at the edge of the grain boundary denoted by the green dotted line in Figure 3c. Periodic NiO structure inside a grain is shown on the right side of the yellow line while broken periodicity inside a grain boundary is observed on the left one. It was reported that such structural characteristic of grain boundary region in NiO resulted from missing oxygen ions and formation of metallic Ni defects.[25] In contrast, no structural changes were observed in cross-sectional HR-TEM data for 30% NiO film before and after applying $V_{threshold}$ (see Figure S3 in the Supporting Information).

Panels a and b in Figure 4 show threshold switching characteristics of the 30% NiO at room temperature and 5% Li-NiO at temperatures from 30 to 130 °C, respectively. The lines show data measured by double voltage sweeps using different compliance current (CC) values while the red triangles denote data obtained by single current sweep. The voltage is swept from 0 to 3 V and vice versa using CC to limit the current. It is interesting that V_{hold} reduces as the CC increases in double voltage sweeps. We have confirmed such tendency at different voltage sweep rates of 1.2 V/s and 31.25 V/s (see Figure S4 in the Supporting Information). The voltage sweep data imply that LRS of threshold switching NiO becomes more stable under higher CC. As seen in Figure 4b, NiO retains threshold switching above 100 °C in contrast to VO_2 which shows a semiconductor metal transition at 65−68 °C.[26,27]

Additional analysis has been done using a current sweep to determine relationship between threshold switching and current allowed. As shown in Figure 4, both current and voltage sweeps follow the same curve prior to reaching $V_{threshold}$ at around 2.4 V.

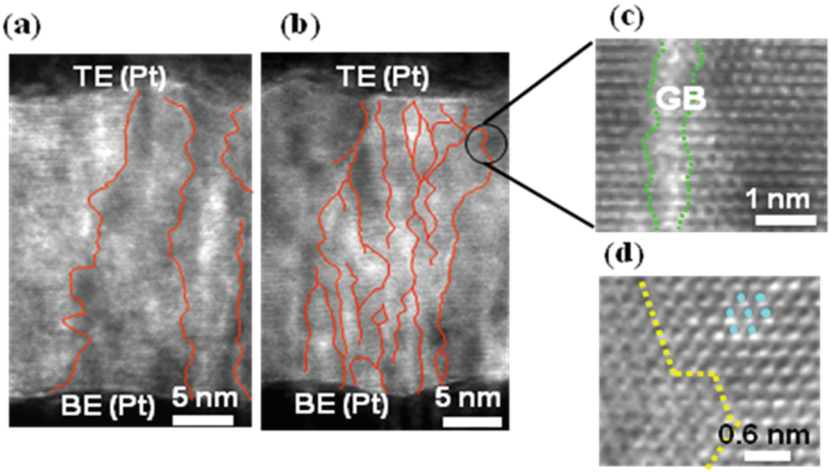


Figure 3. HR-TEM analyses of structural changes in memory switching NiO. Cross-sectional HR-TEM images of 5% NiO films (a) before and (b) after applying V_{set}. (c) An enlarged HR-TEM image near a grain boundary in Figure 3b. (d) Atomic image obtained near edge between grain and grain boundary in Figure 3c.

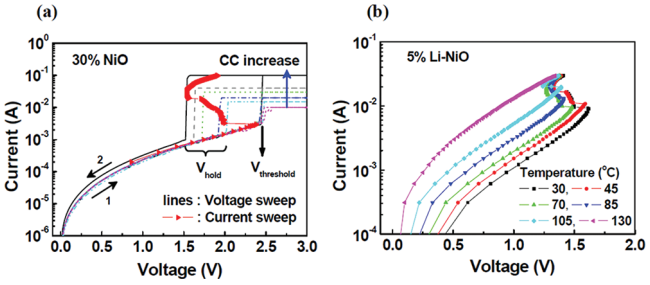


Figure 4. Threshold switching characteristics. a) Data obtained from double voltage sweep measurements (0 V → 3 V → 0 V) under various compliance currents and single current sweep measurement (0.1 mA → 100 mA) for 30% NiO. (b) Data obtained from single current sweep measurement (0.1 mA → 30 mA) for 5% Li-NiO sample at temperatures from 30 to 130 °C.

However, voltage decreases from $V_{threshold}$ (2.4 V) to V_{hold} (1.5 V) as applied current increases indicating current controlled negative differential resistance. In the negative differential resistance region, self-sustaining current channels are enhanced with applied current. From the voltage and current sweep results, we can argue that characteristics of such channels depend highly on the current allowed during switching. These behaviors indicate that the threshold switching characteristics can be controlled by the total amount of current passing through the device.[28,29] Threshold switching is believed to be the results of the collapse of the electric field in the material due to enhancement of either carriers, mobility or off equilibrium by external field.[20]

From hall measurements, hole carrier concentration was determined to be ~1.05×10^{18} cm^{-3} for 30% NiO, ~4.1×10^{18} cm^{-3} for 5% Li-NiO, and ~2.1×10^{16} cm^{-3} for 5% NiO. These values are also close to approximate values determined by the measured conductivities of the samples as shown in Figure 2a. Elipsometry analyses also showed that refractive index of 30% NiO or 5% Li-NiO was higher than that of 5% NiO indicating higher free carrier density of 30% NiO or 5% Li-NiO (see Figure S5a in the Supporting Information). Above 3 eV, extinction coefficient showed similar trend to refraction index. However, below 3 eV, extinction coefficient of the 5% NiO became larger than that of 30% NiO or 5% Li-NiO implying higher defect density of the 5% NiO (see Figure S5b in the Supporting Information). Since more stable threshold switching has been observed under higher current, it is expected that threshold switching is more easily induced in a material with higher carrier concentration. Therefore, the appearance of threshold switching for samples with higher hole carrier concentration can be explained. In such samples, high current flows through bulk materials and can change the electronic states without structural change resulting in volatile threshold switching. However, in the 5% NiO sample with lower hole carrier concentration, charge carrier mainly flow through local weak region, such as grain boundary with metallic Ni. High voltage such as V_{set} can induce evolution and increase in density of grain boundary as shown in Figure 3a and b resulting in nonvolatile memory switching.

CONCLUSION

In conclusion, we have investigated nonvolatile memory and volatile threshold switching of NiO films with low and high hole carrier concentration, respectively. Nonvolatile memory switching is accompanied by increase in density of grain boundary contrary to volatile threshold switching. Instead, volatile threshold switching is controlled by current passing through NiO film with high hole carrier concentration. It is revealed that such NiO films are scalable to ~30 nm feature size and compatible with MLC technology. A simple stacking unit consisting of all NiO storage and switch elements shows typical operation of a random access nonvolatile memory device. The requirements for terabit class nonvolatile memory, such as scalability, multilevel, and stackability, have been met by all NiO storage and switch elements.

ASSOCIATED CONTENT

Supporting Information. Further experimental details, electrical measurements, SEM images, cross-sectional HR-TEM images, and sweep rates of the threshold switching. This material is available free of charge via the Internet at http://pubs.acs.org.

AUTHOR INFORMATION

Corresponding Author

*E-mail: myoungjae.lee@samsung.com (M.-J.L.); baehpark@konkuk.ac.kr (B.-H.P.).

ACKNOWLEDGMENT

This work was supported by the KOSEF NRL Program grant funded by the Korea government MEST (2008-0060004), WCU program through the NRF funded by the MEST (R31-2008-000-10057-0), Seoul R&BD Program (WR090671), and NRF grant funded by the Korea MEST (Quantum Metamaterials Research Center, R11-2008-053-03002-0).

REFERENCES

(1) *International Technology Roadmap for Semiconductors* (ITRS), ITRS 2009 edition.

(2) Liu, S. Q.; Wu, N. J.; Ignatiev, A. *Appl. Phys. Lett.* **2000**, *76*, 2749–2751.

(3) Lee, M.-J.; Han, S. W.; Jeon, S. H.; Park, B. H.; Kang, B. S.; Ahn, S. E.; Kim, K. H.; Lee, C. B.; Kim, C. J.; Yoo, I.-K.; Seo, D. H.; Li, X.-S.; Park, J.-B.; Lee, J.-H.; Park, Y. S. *Nano Lett.* **2009**, *9*, 1476–1481.

(4) Shima, H.; Takano, F.; Akinaga, H.; Tamai, Y.; Inoue, I. H.; Takagi, H. *Appl. Phys. Lett.* **2007**, *91*, 012901.

(5) Allwood, D. A.; Xiong, G.; Faulkner, C. C.; Atkinson, D.; Petit, D.; Cowburn, R. P. *Science* **2005**, *309*, 1688–1692.

(6) Herner, S. B.; Bandyopadhyay, A.; Dunton, S. V.; Eckert, V.; Gu, J.; Hsia, K. J.; Hu, S.; Jahn, C.; Kidwell, D.; Konevecki, M.; Mahajani, M.; Park, K.; Petti, C.; Radigan, S. R.; Raghuram, U.; Vienna, J.; Vyvoda, M. A.; Rotenberg, E.; Bostwick, A.; Ohta, T.; McChesney, J. L.; Seyller, T.; Horn, K. *IEEE Electron Device Lett.* **2004**, *25*, 271–273.

(7) Kang, B. S.; Ahn, S. E.; Lee, M.-J.; Stefanovich, G.; Kim, K. H.; Xianyu, W. X.; Lee, C. B.; Park, Y. S.; Baek, I. G.; Park, B. H. *Adv. Mater.* **2008**, *20*, 3066–3069.

(8) Strukov, D. B.; Snider, G. S.; Stewart, D. R.; Williams, R. S. *Nature* **2008**, *453*, 80.

(9) Lee, M.-J.; Kim, S. I.; Lee., C. B.; Yin, H.; Ahn, S. E.; Kang, B. S.; Kim, K. H.; Park, J. C.; Kim, C. J.; Song, I. H.; Kim, S. W.; Stefanovich, G.; Lee, J. H.; Chung, S. J.; Kim, Y. H.; Park, Y. S. *Adv. Mater.* **2009**, *19*, 1587–1593.

(10) Adler, D.; Shur, M. S.; Silver, M.; Ovshinsky, S. R. *J. Appl. Phys.* **1980**, *51*, 3289–3309.

(11) Bosnell, J. R.; Thomas, C. B. *Solid-State Electron.* **1972**, *15*, 1261–1264.

(12) Seo, S.; Lee., M. J.; Seo, D. H.; Jeoung, E. J.; Suh, D.-S.; Joung, Y. S.; Yoo, I. K.; Hwang, I. R.; Kim, S. H.; Byun, I. S.; Kim, J.-S.; Choi, J. S.; Park, B. H. *Appl. Phys. Lett.* **2004**, *85*, 5655.

(13) Rozenberg, M. J.; Inoue, I. H.; Sanchez, M. J. *Phys. Rev. Lett.* **2004**, *92*, 178302.

(14) Waser, R.; Aono, M. *Nat. Mater.* **2007**, *6*, 833–840.

(15) Lee, M. J.; Park, Y.; Ahn, S. E.; Kang, B. S.; Lee, C. B.; Kim, K. H.; Xianyu, W. X.; Yoo, I. K.; Lee, J. H.; Chung, S. J.; Kim, Y. H.; Lee, C. S.; Choi, K. N.; Chung, K. S. *J. Appl. Phys.* **2008**, *103*, 013706.

(16) Aziza, M. S.; Abdel-Wahabb, F.; Mostafac, A. G.; El-Agwany, E. M. *Mater. Chem. Physt.* **2005**, *91*, 532–537.

(17) Street, R. A.; Mott, N. F. *Phys. Rev. Lett.* **1975**, *35*, 1293–1296.

(18) Lee, M.-J; Park, Y.; Suh, D.-S.; Lee, E.-H.; Seo, S.; Kim, D.-C.; Jung, R.; Kang, B.-S.; Ahn, S.-E.; Lee, C. B.; Seo, D. H.; Cha, Y.-K.; Yoo, I.-K.; Kim, J.-S.; Park, B. H. *Adv. Mater.* **2007**, *19*, 3919–3923.

(19) Chang, S. H.; Lee, J. S.; Chae, S. C.; Lee, S. B.; Liu, C.; Kahng, B.; Kim, D.-W.; Noh, T. W. *Phys. Rev. Lett.* **2009**, *102*, 026801.

(20) Ielmini, D. *Phys. Rev. B* **2008**, *78*, 035308.

(21) Baek, I. G.; Lee, M. S.; Seo, S.; Lee, M. J.; Seo, D. H.; Suh, D.-S.; Park, J. C.; Park, S. O.; Kim, H. S.; Yoo, I. K.; Chung, U.-I.; Moon, J. T. *Tech. Dig. —Int. Electron Devices Meet.* **2004**, 587.

(22) Pershin, Y. V.; Ventra, M. Di *Advanced in Phys.* **2011**, *60*, 145–227.

(23) Ielmini, D.; Nardi, F.; Cagli, C. *Appl. Phys. Lett.* **2010**, *96*, 053503.

(24) Son, M.; Lee, J.; Park, J.; Shin, J.; Choi, G.; Jung, S.; Lee, W.; Kim, S.; Park, S.; Hwang, H. *IEEE Electron Device Lett.* **2011**, DOI: 10.1109/LED.2011.2163697.

(25) Park, G.-S.; Li, X.-S.; Kim, D.-C.; Jung, R.-J.; Lee, M.-J.; Seo, S. *Appl. Phys. Lett.* **2007**, *91*, 222103.

(26) Sahana, B.; Subbanna, G. N.; Shivashankar, S. A. *J. Appl. Phys.* **2002**, *92*, 6495–6504.

(27) Cho, C.-R.; Cho, S.; Vadim, S.; Jung, R.; Yoo, I. K. *Thin Solid Films* **2006**, *495*, 375–379.

(28) Emin, D. *Phys. Rev. B* **2006**, *74*, 035206.

(29) Haberland, D. R.; Stiegler, H. *J. Non-Cryst. Solids* **1972**, *8—10*, 408–414.